IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, line 5 with the following paragraphs:

This application is related to co-pending U.S. Patent Application No. ~~(Attorney Docket No. CALMP014)~~ 09/496,897, entitled "DC Control Of A Multilevel Signal," filed ~~concurrently herewith~~ February 2, 2000, now U.S. Patent No. 6,604,219, issued August 5, 2003, which is incorporated herein by reference for all purposes and U.S. Patent Application No. ~~(Attorney Docket No. CALMP013~~ 09/496,387, entitled "Generating A Multilevel Calibration Sequence For Precompensation," filed ~~concurrently herewith~~ February 2, 2000, now U.S. Patent No. 6,608,807, issued August 19, 2003, which is incorporated herein by reference for all purposes.

Please replace the paragraph beginning on page 10, line 9 with the following paragraph:

Figure 2 is a block diagram illustrating a write compensation system such as may be included in data compensator 122 of Figure 1B.

Please replace the paragraph beginning on page 11, line 4 with the following paragraph:

Figure 6B is a graph illustrating an example of ~~such a relationship and~~ the typical nonlinear response of an optical media to a write strategy parameter.

Please replace the paragraph beginning on page 12, line 14 with the following paragraph:

In one embodiment, this invention applies to the methods of writing marks on a phase change material as described in United States Patent Application No. 09/373,916, ~~Attorney Docket No. CALMP007,~~ filed August 12, 1999, entitled "High Density Data Write Strategy" which is herein incorporated by reference, hereinafter O'Neill et. al. As described therein, marks can be written in a manner such that their size can be less than the size of the focused spot of a writing laser. By forming marks smaller than the reading laser beam, the reflectivity of a region of material can be varied with great precision. The reflectivity of a region is controlled by varying the relative amount of material in crystalline and amorphous phases. The total amount of crystalline and amorphous material in a region is controlled by creating marks of various sizes or shapes. In turn, the mark size and shape is controlled by placing the leading and trailing edges of laser

pulses such that the timing of a second laser pulse further modifies the region of material irradiated by a first pulse. Additional modification of the mark size and shape results from controlling the time course of the laser power during the pulse.

Please replace the paragraph beginning on page 15, line 2 with the following paragraph:

Figure 2 is a block diagram illustrating a write compensation system such as may be included in data compensator 122 of Figure 1B. A test pattern that is created by a test data generator 202 is passed to a data formatter 204 where the data is organized and various calibration and control patterns are added. The resulting formatted test pattern is separately passed through the physical channel (writer 206 and reader 208) and through a channel model 210.

Please replace the paragraph beginning on page 16, line 9 with the following paragraph:

Various control sequences may be added to the test pattern of interest to aid in the recovery of data. The most significant of these types of control sequences include synchronization marks, timing and alignment sequences, and automatic-gain-control (AGC) sequences such as are described in United States Patent Application No. 09/253,808, ~~Attorney Docket~~

~~No. CALMP009,~~ filed February 18, 1999, entitled "Architecture For Reading A Multi-Level Signal From An Optical Disc", now U.S. Patent No. 6,275,458, issued August 14, 2001, which is herein incorporated by reference. Figure 3 is a diagram illustrating a more detailed breakdown of data formatter 204 shown in Figure 2. A data generator 302 outputs data to a sync mark insertion block 304. The output of sync mark insertion block 304 is input to a timing sequence insertion block 306. The output of timing sequence insertion block 306 is input to a AGC sequence insertion block 308.

Please replace the paragraph beginning on page 17, line 16 with the following paragraph:

The purpose of the type-I pattern is to sample reflectivity values resulting from a particular choice of write strategy parameters. The resulting data is then used by the write strategy calculator to initialize the write strategy matrix. An example of a type-I pattern for the write strategies outlined in United States Patent Application No. 09/373,916, ~~Attorney Docket No. CALMP007,~~ filed August 12, 1999, entitled "High Density Data Write Strategy" which is herein incorporated by reference, hereinafter O'Neill et. al. is given below. In the example given, the laser power associated with each pulse is fixed and the pulse width is chosen as the write strategy parameter that is varied by the input data to control the reflectivity of a mark.

Please replace the paragraph beginning on page 18, line 8 with the following paragraph:

Figure 6C is a graph illustrating an example of a sequential scan through pulse width and the resulting changes in reflectivity. The type-I test pattern "T1" that was used in this example can be represented by a series of integers representing pulse width: 1,2,3,4,5,6,7,8,9,10,11,12,4,0,4 where 0= laser off. The last elements of the sequence, ~~4,04~~ 4,0,4, are included as a sync mark.

Please replace the paragraph beginning on page 21, line 7 with the following paragraph:

In another embodiment, the type-II pattern is generated using the shift register sequences described in U.S. Patent Application No. ~~_____(Attorney Docket No. CALMP013)~~ 09/496,387, filed ~~concurrently herewith~~ February 2, 2000, entitled "Generating A Multilevel Calibration Sequence For Precompensation", now U.S. Patent No. 6,604,219, issued August 5, 2003. The shift register sequences are easier to generate in some cases than the deBruijn sequences. In some embodiments, the type 1 and type 2 patterns may be altered to reduce low frequency signal content as is described in United States Patent Application No. ~~_____(Attorney Docket No. CALMP014)~~ 09/496,897, filed ~~concurrently herewith~~ February 2, 2000, entitled "DC Control Of A

Multilevel Signal", now U.S. Patent No. 6,608,807, issued August 19, 2003. In another embodiment, a random or pseudo-random sequence of data is used and a DC control algorithm is applied to the sequence. The length is chosen to be sufficient such that all subsequences of interest are sampled with adequate statistics.

Please replace the paragraph beginning on page 26, line 5 with the following paragraph:

The structure of the write strategy matrix is general purpose and can be applied to other write strategies without loss of function. The write strategies contained in United States Patent Application No. 09/373,916, ~~Attorney Docket No. CALMP007,~~ filed August 12, 1999, entitled "High Density Data Write Strategy" which is herein incorporated by reference, hereinafter O'Neill et. al. are shown as examples only. The write compensation algorithm described here can be applied to write strategies and write strategy parameters other than the ones mentioned as examples.

Please replace the paragraph beginning on page 26, line 20 with the following paragraph:

In one embodiment, a fully programmable write laser control signal is generated using a multiplexer that selects inputs from different delay lines for the purpose of precisely adjusting the timing of write signal transitions derived from the multiplexer

output such as is described in United States Patent Application No. 09/393,208, ~~attorney docket no. CALMP012,~~ filed September 9, 1999, entitled "Programmable Write Signal Generator", now U.S. Patent No. 6,269,060, issued July 13, 2001, which is herein incorporated by reference. The delay lines may be obtained by using one or more delay lock loops referenced to an external clock to derive delay control voltages for delay cells. The delays produced by the delay cells are precisely defined fractions of the external clock period and are independent of fluctuation in temperature or power supply voltage. The derived delay voltages are input to delay stages to precisely generate delays for the input delay lines. The delay line corresponding to the exact desired delay can be selected by the multiplexer.

Please replace the paragraph beginning on page 32, line 5 with the following paragraph:

The write strategy calculator determines a set of write strategy parameters that correspond to input data subsequences. The write strategy parameters determine laser control instructions such that the relationship between the input data sequence and the recovered data is close to the specified target. As mentioned above, the target may be either fixed or dynamic. In addition to this function, the write strategy calculator must perform a number of supporting operations including write strategy matrix

initialization, data alignment, and determining when and how to exit the write compensation procedure.

Please replace the paragraph beginning on page 33, line 20 with the following paragraph:

In the study of numerical methods, algorithms are generally classified as direct or iterative. In one embodiment, the method of computing a final write strategy matrix is a ~~combinations~~ combination of direct and iterative methods in that it is an iterative improvement to a direct calculation. The direct calculation is discussed in the initialization section, and the iterative calculation is discussed in the subsequent iteration and control section.

Please replace the paragraph beginning on page 35, line 10 with the following paragraph:

Once the relationship between the write strategy parameter and the reflectivity is measured, the maximum and minimum values of reflectivity are determined (points R_{max} and R_{min}). Two new points X and Y are defined by moving up from the minimum reflectivity (point Y) and down from the maximum reflectivity (point X) by a small fraction (in one embodiment about 10%) of the full dynamic range (R_{max} - R_{min}). A "working" dynamic range DR_w is defined by these two new points: DR_w=X-Y. This working dynamic

range is smaller than the full DR (R_{max} - R_{min}) to allow the write compensation procedure to adjust the points of maximum and minimum reflectivity either up or down.

Please replace the paragraph beginning on page 42, line 13 with the following paragraph:

In one embodiment, the entire formatted type-II pattern is passed through the level placement matrix (LPM) and loaded into a buffer_A. Because the type-II pattern is internally generated, a pointer to the beginning of the type-II pattern in buffer_A can be set by construction. The sampled output of the read-channel front end is then loaded into a buffer_B. In some embodiments, the read data may be sampled at a rate other ~~that~~ than the data cell frequency. In such a case, the size of buffer_B is scaled accordingly. A pointer into buffer_B is subsequently set to point to the beginning of the type-II pattern by locating a timing-zero-locator (TZL) sequence. As discussed above, this sequence is a pseudo-random sequence that can be used by a circuit or algorithm to locate the beginning of a formatted block of data containing the type-II pattern. In other embodiments, the output of an "Software Iteration write strategy matrix" may substitute for the read channel source.

Please replace the paragraph beginning on page 43, line 14 with the following paragraph:

The output of the pattern aligner (pointers to the beginning of the patterns in each of the filled buffers A and B) forms the input to the channel model updater. Upon entry into the channel model updater, the associated channel model parameters are loaded (e.g., number and values of the initial filter taps). The type of channel model (fixed or dynamic) determines the type of parameters that are loaded. No update to the channel model is necessary for fixed channel models, so ~~the~~ a buffer_C containing the channel's target values is simply filled.